
HERMES

Hermes

DDC/DUC
HF transceiver

from

OpenHPSDR

an
(UNOFFICIAL)
introduction for new learners

This document, diagrams, illustrations and all written material is presented for entertainment purposes only. This is my personal effort to share my excitement about the Hermes OpenHPSDR transceiver project.

This document was NOT sponsored or approved by Dave KVØS and OpenHPSDR.org it is my personal UNOFFICIAL introduction.

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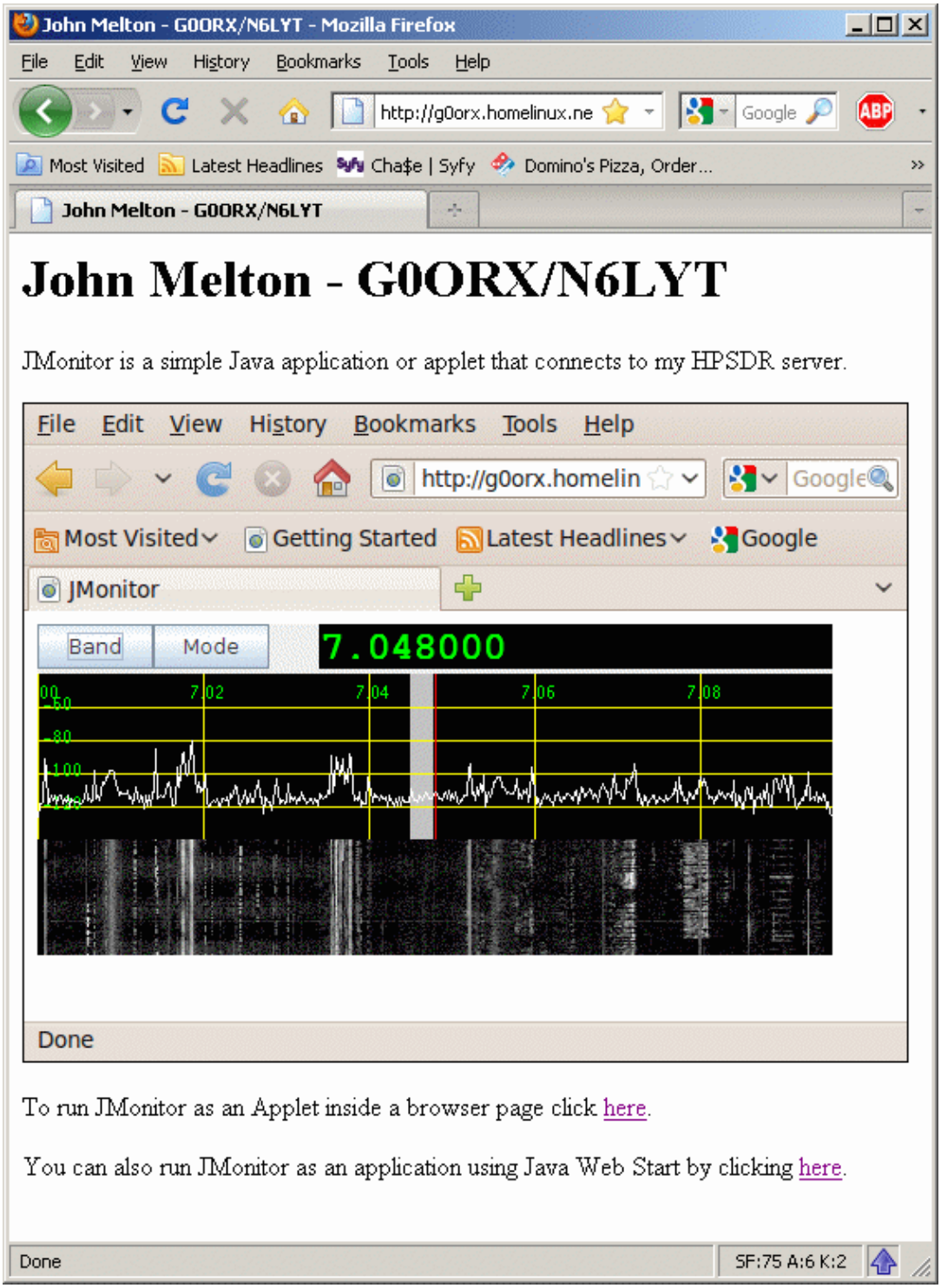
HIGHLY RECOMMENDED FOR ALL NEW DDC LEARNERS

To learn all about Digital Down Converter technology, **please purchase DVD #6** from (Amateur Radio Video News) in which Phil Harman VK6APH teaches us the practical details from his wonderful presentation at ARRL/TAPR DCC-2008. The DVD consists of 4 hours of high quality education in DDC by Phil Harman. The ARVN webpage says:
Software Defined Radio
"Through the Looking Glass"
Phil Harman VK6APH leads you on an entertaining, detailed trip through the design of the Mercury SDR receiver. With the A/D converter preceded only by a bandpass filter, Mercury does everything in software, at a price hams can afford. It is the leading edge in ham radio technology.

http://www.arvideonews.com/dcc2008/

First web browser java based Jmonitor
experiment and demonstration
by
John Melton GØORX/N6LYT
February 2010



Abstract

OpenHPSDR Hermes is a complex Software Defined Radio (SDR), high density single board HF transceiver requiring only an antenna, power supply, and a Industry Standard TCP/IP network Ethernet 100BT/1000BT connection to a computer. Hermes exploits the benefits of digitally processing **I** (in phase) and **Q** (quadrature) signals in the digital domain and DSP for demodulation in the Industry Standard TCP/IP network Ethernet 100BT/1000BT connected computer.

Software support for Hermes is currently PowerSDR(R), K.I.S.S. Konsole, ghpsdr3, QtRadio, and Heterodyne for the MAC. It is anticipated that the proposed Athena Software Framework will point toward a client/server architecture in the future.

The *OpenHPSDR Hermes* contains a full Digital Down Conversion (DDC) receiver, and a Digital Up Conversion (DUC) transmitter. The combination yields an exciting new HF transceiver (10kHz to 55MHz Rx and 500kHz to 54MHz Tx). The concept for Hermes was introduced by Kevin Wheatley M0KHZ through the collaboration of the HPSDR community. Hermes is now a reality. Hermes Team list on page 12.

Hermes is based on the successful OpenHPSDR Atlas + PennyLane (Tx) + Mercury(Rx) + Metis (Ozy-II) (control) designs. Kevin proposed that OpenHPSDR could combine the receiver and transmitter processing requirements into a single FPGA on a single PCB in a compact design at a lower cost.

The precision of mathematical processing DDC/DUC is new in Ham Radio, but relies on the underlying I/Q Phasing method which has been understood and used for 5 decades. DDC/DUC was made possible by the reduction in price and dramatic increase in performance of Analog to Digital Conversion (ADC) chips for the cell phone and other communication industries.

The Hermes concept is to use the state-of-the-art design to bring RF signals from the analog domain directly to the digital domain for computer processing in receive, and similarly using a DAC path in transmit.

Digital processing of I and Q signals has proven it's ability to surpass conventional analog designs while delivering exciting new communication technologies.

Hermes was the great Messenger of the gods in Greek mythology as well as an Olympian god.

The overall transceiver concept is explained here:
Hermes Wiki http://openhpsdr.org/wiki/index.php?title=HERMES

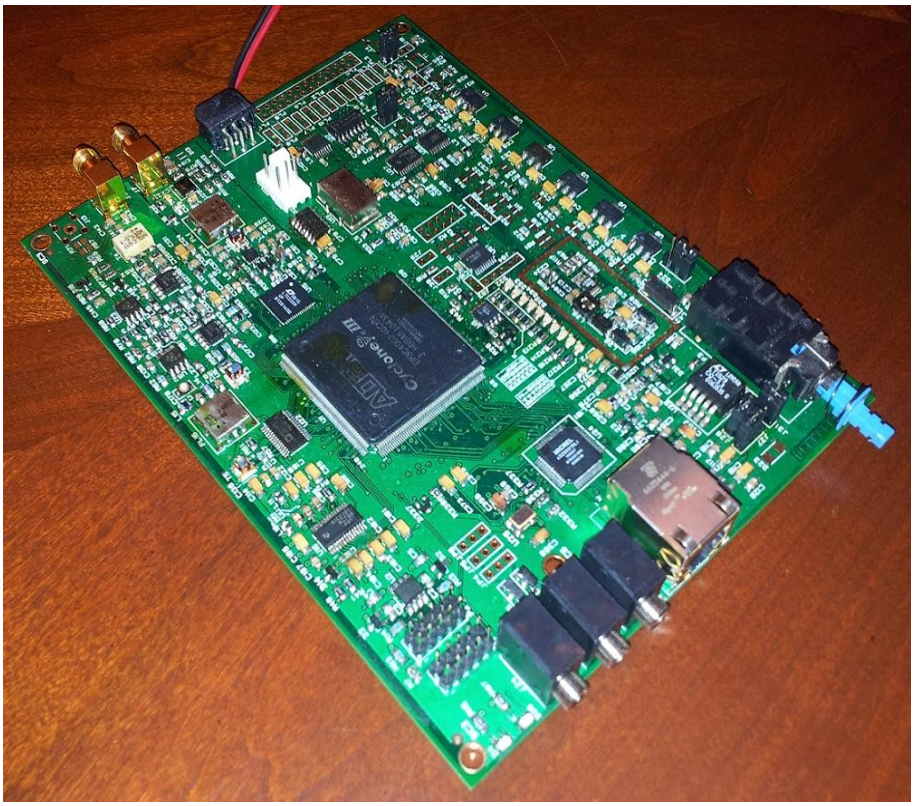
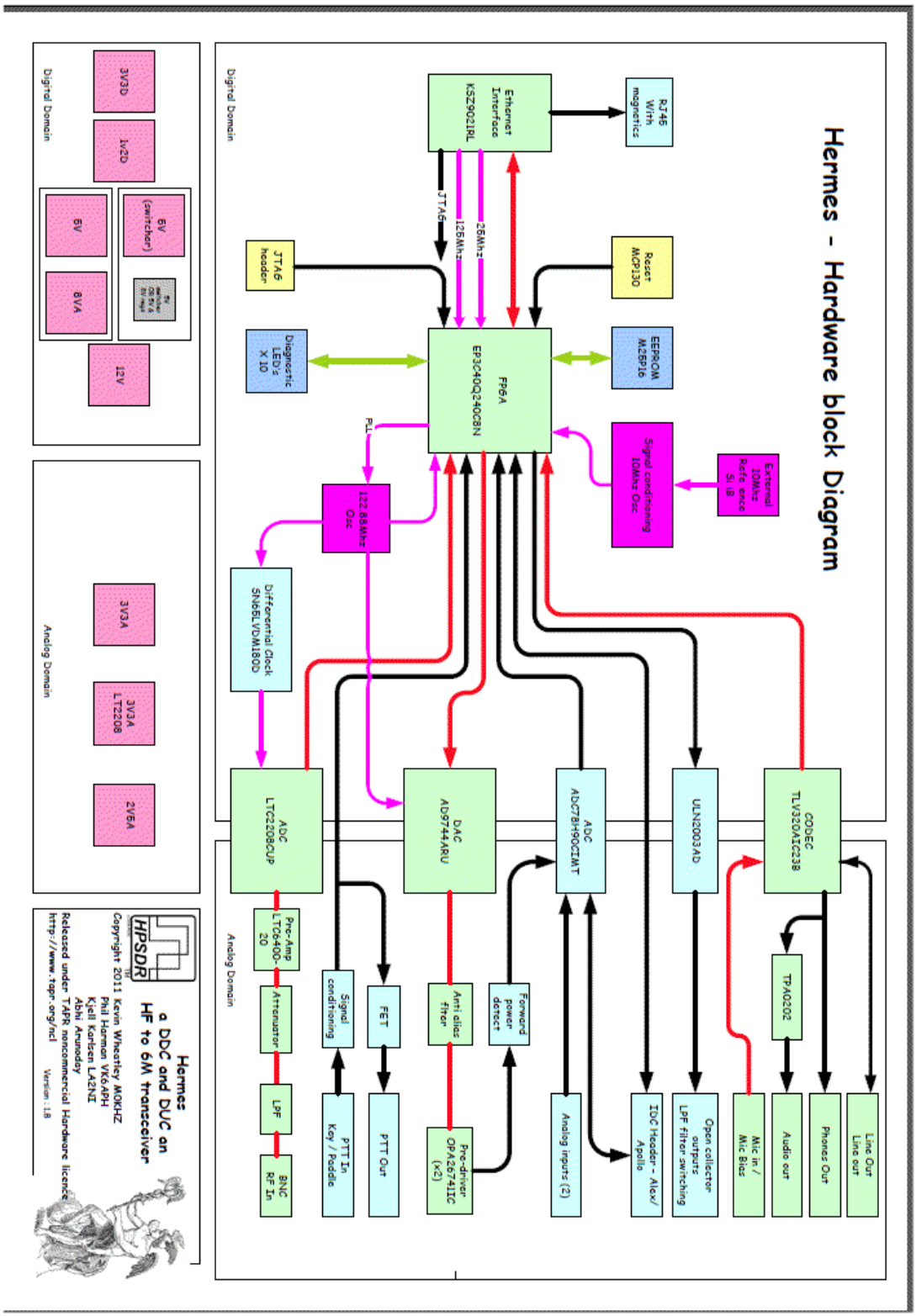


photo courtesy *Abhi Arunoday*

PowerSDR(R)
K.I.S.S. Konsole(GPL)
Heterodyne (GPL for MAC)

and new software from

John Melton
GØORX/N6LYT



Hermes block diagram
courtesy Kevin Wheatley M0KHZ

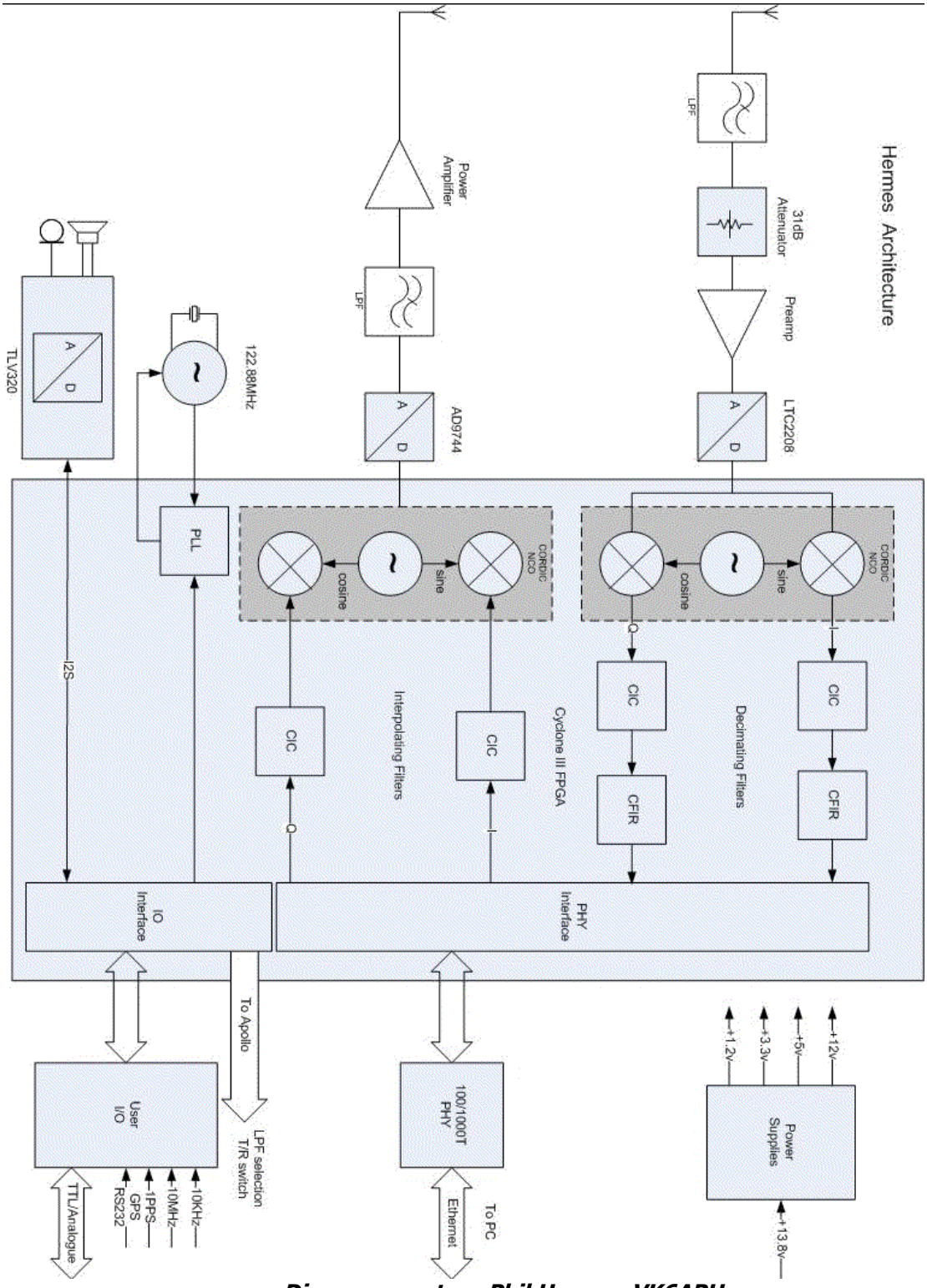


Diagram courtesy Phil Harman VK6APH

2011 TCP/IP interface

Ham Radio is enjoying a period of tremendous change, adaptation, and evolution. We have left a legacy of rigs that you repair yourself and grown to rigs you can enhance yourself; from rigs you build out of parts, to rigs you build out of functional blocks; from rigs that are self contained trophy's of bent aluminum, to rigs that beat with an invisible heart of software. OpenHPSDR has given us Hermes as a link to this new era of **Software Defined Ham Radio.**

The OpenHPSDR Hermes transceiver is the mechanical base on which you can build your dream software defined radio. In the future, with the Athena software framework, Hermes software can be morphed into any display you desire, on your favorite brand of computer.

Now it is up to us. We are no longer tied to the design, profit goals, and priorities of a manufacturer. You can dream about exotic and unique SWL features with imported European MF databases. You can dream about how you would layout multiple panadapters wiggling their FFT displays in front of your eager eyes. You can dream about the best Noise Blanker or Manual Notch Filter **and** you can homebrew any of the solutions.

Are you ready for the challenges of the software defined era of Ham Radio?

Introduction: There have been three significant generations of I and Q signal processing for Ham Radio; (a) Phasing Method, (b) QSD method, and (c) the new DDC/DUC Method.

CE100v phasing exciter

(a) The *first generation* phasing method was successfully implemented in various Ham gear in the late 1950's. "I" in phase and "Q" quadrature signals were of the highest analog quality in the advanced Central Electronics CE-100v. Many proud owners of the CE-100 and 200 models can be heard operating them on the bands today. A good reference to 1960 SSB is: http://en.wikipedia.org/wiki/Single-sideband_modulation#Weaver_modulator

(b) The *second generation* Quadrature Sampling Detectors (QSD) and mixers were popularized by Dan Tayloe N7VE beginning in 1998. The first QSD Ham rig was introduced by Gerald Youngblood K5SDR in the his SDR-1000 QEX articles in 2002. The Flex-Radio website has a full collection of Gerald's articles and hundreds of other supportive technical materials about the modern FLEX-5000 series equipment.

FLEX-5000a

Tony KB9YIG has miniaturized and simplified a QSD design. Tony has sold more than 11,000 of the inexpensive SoftRock QSD kits to a world-wide audience.

(c) The third generation of phasing modulation and demodulation (I and Q) is now a reality as we follow the introduction of affordable high-speed analog to digital conversion integrated circuits. These amazing ADC chips, like the LTC2208 (discussed below), are available to the experimenter to create new Software Defined Radios. The OpenHPSDR and Hermes projects are state-of-the-art implementations that follows the true spirit of Ham Radio design where everything about the system is open and shared.

http://openhpsdr.org/wiki/index.php?title=FAQ

Description

The HPSDR and Hermes transceiver follows the OpenHPSDR Mercury/PennyLane/Ozy as one of the most advanced digital (DDC/DUC) transceivers available for experimentation. Every chip and circuit has been chosen to offer the highest performance and value at an affordable cost. The DDC Hermes receiver features a Linear Technology LTC2208 16 bit, 130 MSPS Analog Digital Converter (ADC) and an Altera EP3C40Q Cyclone III FPGA. Connectivity to the PC is through a high speed Industry Standard TCP/IP network Ethernet 100BT/1000BT interface. The general coverage Mercury receiver covers 10kHz through 55MHz in its standard configuration and can probably be used in under sampling applications in the VHF/UHF spectrum. The transmitter covers traditional HF Ham bands as defined by each ITU Region.

The Hermes transceiver uses approximately 50% of the FPGA capacity allowing extra room for future expansion. Multiple independent receiver chains sharing the ADC anywhere within the 10kHz - 55 MHz range is one possibility. Three independent receivers have already been demonstrated by John Melton GØORX/N6LYT, and 7 receivers have been demonstrated by Alex VE3NEA.

All the features of the Hermes transceiver benefited from the HPSDR Mercury + PennyLane + Ozy + Atlas project. Each new feature was selected to set it apart from any other DDC/DUC based software defined radios. Hermes transceiver is not a black-box design. The Hermes transceiver is OPEN SOURCE. Open Source means that you can view, change, improve, and experiment with what is inside. The ability to see the internals of both OpenHPSDR Hermes and software programming gives you a special opportunity to study how a sophisticated DDC/DUC transceiver works.

In the old-days you could study a schematic, now you can study schematics AND dissect the software heart of the OpenHPSDR Hermes. Since the majority of the digital functionality is within the FPGA and computer software, a new, updated radio is only a download away.

The manufacturer for Hermes is expected to be announced shortly.

Who are the contributing members to the Hermes project?

THANK YOU each for the wonderful gift you have shared with us all

- Kevin Wheatley M0KHZ who conceived the Hermes and is the Project Lead
- Abhi Arunoday PCB layout
- Phil Harman - VK6APH - Software & hardware development, especially the brain wave for maintaining full DAC bits while reducing power.
- Bill Tracey - KD5TFD - Component sourcing and kitting
- Lyle Johnson - KK7P - significant contributor with PennyLane Tx hardware development
- Scotty Cowling - WA2DFI – Parts procurement
- Graham - KE9H - Hermes PA improvements
- Plus numerous other contributors via the OpenHPSDR reflector.
- Apollo, a companion 20W PA, LPF and ATU, was conceived by Kjell Karlsen – LA2NI

OpenHPSDR Hermes: **http://en.wikipedia.org/wiki/Hermes** The "Hermes" project that is part of the **H**igh **P**erformance **S**oftware **D**efined **R**adio group's ensemble of boards used in the original Atlas based backplane. The OpenHPSDR home is here: http://openhpsdr.org/

DDC: DDC is the abbreviation for the term Digital Down Conversion. DDC receivers are able to finally fulfill the dream that has been expressed in Ham Radio magazines for 50 years – to move the digital processing of analog RF information from the back of the receiver chain closer to the antenna. OpenHPSDR has created the Hermes and Mercury receivers to accomplish exactly that goal. The chip in this case is a very fast Analog to Digital conversion device from Linear Technologies the LTC2208 (more information below). The Hermes transceiver is designed to be supplemented by bandpass, attenuation, or pre-amp and PA circuits from the Alex or Apollo projects:

- Frequency Range: 10 kHz to 55 MHz Rx and 500Khz to 54Mhz Tx
- Input Impedance: 50 ohms
- Clipping RF Level: +9 dBm (~S9 + 80db)
- Maximum Display Bandwidth: 50MHz
- ADC Sampling Clock: 122.88 MHz (can be phase locked to an external 10MHz reference)
- I/Q Image Rejection: >110 dB
- MDS (500 Hz): -135 dBm @ 14 MHz (Preamp on)
- IP3: +50 dBm
- BDR: 125 dB
- Voltage: 12 - 15 VDC, 4A fused
- Current Draw: approx 500 mA (typ.)
- LEDS: Power, FPGA loaded , Power Supplies (internal)
- Dimensions: 100x 160mm (3.299" x 3.940") (Eurocard size)

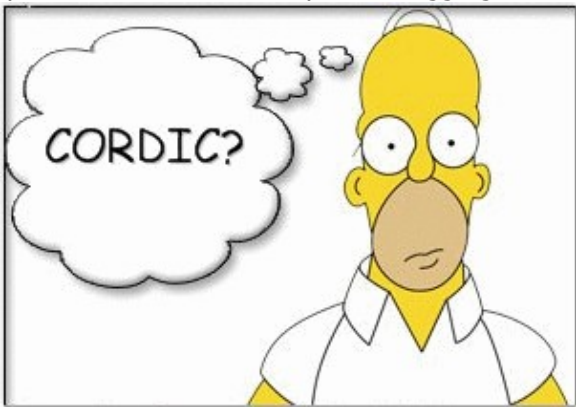
LTC2208: The Linear Technologies LTC2208 is a high speed, state-of-the-art, Analog to Digital conversion integrated circuit. The specifications for the LTC2208 (and it's cousin the 2209) can be found on the Linear Technologies website. The LTC2208 is just the beginning of the most exciting new era in Ham Radio. It offers us the ability to convert analog RF signals in the 10Khz to 55Mhz range to digital signals. The conversions happen in the OpenHPSDR Hermes at the blazing rate of 122.88 Million Samples Per Second!

I realize that this is a difficult concept to grasp. Many hams have grown up in an Analog world. I am sure we all will all enjoy reading the OpenHPSDR explanations and analogies about how the Hermes transceiver architecture relates to designs that we understand. Phil Harman VK6APH has written many articles for the RSGB and was selected as the author for their SDR chapter in the 10th edition RSGB Handbook. In cooperation with TAPR, Gary KN4AQ offers DVD's with the presentation that Phil gave at DCC in 2008 http://www.tapr.org/conf_dcc2008.html. The RSGB material and the DVD's offer new learners the opportunity to gather a good understanding of digital I and Q signal processing and it's wonderful potential use in Ham Radio. There is a great deal of helpful material available on the Internet and from various magazines and books. The ARRL DSP book written by Doug Smith KF6DX has several chapters devoted to various aspects of digital sampling of analog signals. Additionally, the SDR chapter in the 10th edition of the RSGB Handbook (2010) was written by Phil Harman, VK6APH, one of the developers of Hermes.

New Linear Technologies devices allow hams to build affordable equipment that processes the digital representation of the entire RF spectrum throughout the HF ham bands (.05Mhz through 55Mhz). Digital processing gives us extraordinary filters, AGC, MDS, BDR and demodulation that is far beyond any of our older analog circuit designs. The software doesn't change values as equipment heats up and image rejection is always at it's mathematically optimum value.

The ability of the LTC2208 to sustain 122.88 million samples per second couples it to various algebraic and mathematical methods (CORDIC and digital division) that are processed easily inside a miniature logic circuit like the Cyclone-III FPGA. An CW signal on 3.552Mhz appears on the output pins of the LTC2208 among the stream of discrete numerical values ranging from -32768 to +32767 (2^{16}). The LTC2208 converts the RF impulses to decimal values using all sixteen bits of it's internal circuitry. The selection of the LTC2208 16bit part is another illustration of the quality and versatility of the Hermes transceiver architecture.

During every tick of your wall clock, the 2208 presents over one hundred and twenty million samples of the RF spectrum at it's output pins. Each numerical sample is an aggregate value of the RF energy throughout the HF spectrum. It is the job of the logic elements in the Cyclone-III FPGA to create digital I/Q representations of the data, interpret, divide, convert, and prepare the numerical values so that they can be post-processed by the PC Computer software.



The digital I/Q data, once passed to an associated PC via a Industry Standard TCP/IP network Ethernet 100BT/1000BT2 connection, uses PC software to convert the numerical data into human viewable and audible form using the magic of algorithms such as the Fourier transform. The digital signals from the LTC2208 are passed without interference to the Cyclone-III FPGA in a continuous stream where they are processed in real-time and in full duplex.

You may wish to read some of the excellent digital signal processing material available at no cost on the World Wide Web. Terminology such as "time domain" and "frequency domain" will easily be related to oscilloscope patterns that we are all familiar with. In addition to the ARRL and RSGB books, another popular text is The Scientist and Engineer's Guide to Digital Signal Processing By Steven W. Smith, Ph.D.

Altera Cyclone III: The Altera Cyclone-III EP3C40Q is an amazing device. First it is a field programmable set of electronic "gates" that can be combined to work like a very basic (and blazingly fast) computer. The Cyclone-III has the necessary mathematical primitives (such as multipliers) to do the Digital Down Conversion (DDC) and Digital Up Conversion processing simultaneously in parallel.

The receive function of the Cyclone-III is to accept the digital data from the LTC-2208 Analog to Digital conversion chip and hammer it into shape using very sophisticated mathematical tools such as the "CORDIC" algorithm. The result is a stream of I and Q data that is fed to the Industry Standard TCP/IP network Ethernet 100BT/1000BT interface and hence to a general purpose computer for the console display. The Cyclone-III EP3C40Q device has 39,600 logic elements, 1.6MB of RAM memory, and 126 multipliers. The Cyclone-III handbook is over 440 pages of highly technical material. It can be found on the Altera website. The Cyclone-III logic ele-

ments are arranged, directed, and formed into the desired functional blocks by programming in a high level Hardware Description Language called "VHDL" from Verilog.

Computers were first programmed using the most primitive instructions called the "assembler" language. The problem with assembler code is that it is difficult to maintain, modify, and repair. The answer was an explosion of higher level computer languages like Fortran, COBOL, and decades later we have modern languages such as C# and C++. Wikipedia currently lists more then 700 computer languages.

FPGA's are programmed or configured using the Verilog "VHDL" high level language that resembles the popular 'C' computer language. The Verilog compiler prepares logical element links within the Cyclone-III which is reprogrammable at any time. The advantages of Verilog is that it is maintainable, efficient, optimized, can be extended and repaired without unraveling the mysteries of the old opaque assembler style coding. *FPGA coding is NOT trivial*! We owe gratitude and praise for the OpenHPSDR Engineers who shared their skills and coded our FPGA chips.

- The logic elements of the FPGA are configured using Verilog programming. Because the FPGA is such an agile device, the receiver logical elements and algorithms and the transmitter logical elements and algorithms are able to operate concurrently inside the FPGA chip. In receiving there are Decimating Filters and in the transmitter there are Interpolating Filters.
- The Decimating Filters reduce the sample rate from 122.88Msps to 192/96/48ksps as selected by the user. Decimation trades bandscope bandwidth for data rate; the lower data rates are necessary so a slower PC can undertake the rest of the necessary Digital signal processing tasks.
- The Interpolating Filters increase the sample rate from 48ksps to 122.88Msps to comply with the Nyqyist criteria for Digital Up Conversion (DUC) on transmit.

You will find all the low and high level files in the (SVN) repository
svn://svn.openhpsdr.org/

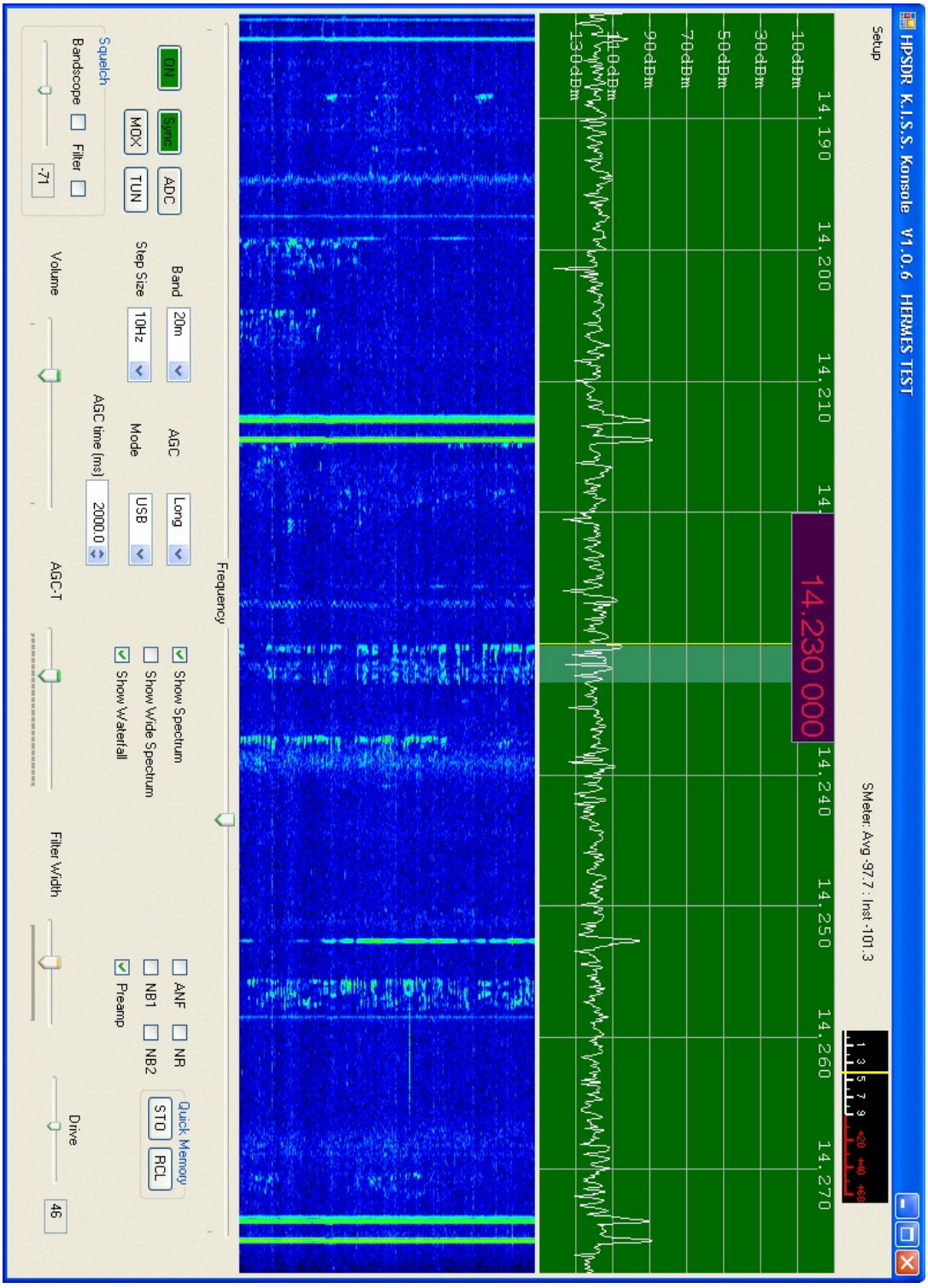
Please refer to appendix A for more information about the CORDIC algorithm and appendix B for an example of Verilog programming.

Hermes Technical Highlights

- Transmit and receiver image rejection > 110dB
- Full duplex operation, any split over entire 160m to 6m range
- Future expansion possible to eight independent receivers using the same antenna
- 500mW RF output on 160 – 6m amateur bands
- Built-in high performance preamp, with a noise floor typically -135dBm in 500Hz
- Software-selectable 31dB input attenuator in 1dB steps
- High performance receiver – same specifications as the HPSDR Mercury receiver (ie Blocking Dynamic Range typically about 125dB)
- FPGA code can be updated via the Industry Standard TCP/IP network Ethernet connection
- Seven user-configurable open-collector outputs, independently selectable per band and Tx/Rx (for relay control, etc - with sequencing via PC code)
- Separate open-collector PTT connection for amplifier control, etc, with sequencer
- Microphone PTT jumper-selectable from tip or ring connection
- Bias for electret microphones via jumper
- Four user-configurable 12 bit analogue inputs (for ALC, SWR etc)
- Three user-configurable digital inputs (for linear amplifier over temperature, etc)
- Optional in-built switch mode power supply – less than xxxmA (receive) from a 13.8V supply
- I2C bus connector for control of external equipment
- Full QSK using the Kiss Konsole software, since digital signal processing is not used in the controlling PC for CW carrier generation
- Low-level transmitter output for transverter use (0dBm) as well as user-selectable output attenuator
- Stereo audio outputs at line and headphone levels
- In-built 1W stereo audio amplifier for directly driving speakers
- Direct, de-bounced connections for a Morse key (straight or iambic) and PTT
- 122.88MHz master clock, which can be phase-locked to an internal 10MHz TCXO or external frequency reference
- Jumper-selectable external frequency reference, with signal processing, to suit numerous GPS-locked 10MHz reference sources
- Direct ribbon cable interface to Apollo 15W power amplifier, low pass filters and automatic ATU.
- Low noise, high efficiency, Switching Power Supply designed by Kjell Karson,LA2NI
- Industry Standard TCP/IP network Ethernet interface supports static, APIP or DHCP IP address
- Hermes responds to ping and ARP requests, auto senses Industry Standard TCP/IP network Ethernet cable connection and connection speed

- Apollo is a combined 15w PA, Low Pass Filter bank and Automatic ATU. The Apollo project is led by Kjell Karlsen LA2NI.
- Eight (8) Layer PCB design with three 1.5vdc oscillators for the most professional, state-of-the-art design available.

New HPSDR **K.I.S.S. Konsole** from Phil Harman VK6APH



for experimenters and new C# learners as well

http://openhpsdr.org/wiki/index.php?title=KISS_Konsole

K.I.S.S (Keep It Simple Stupid) Konsole is a straightforward PC program that will allow beginners in SDR and DSP programming to get their feet wet.

KK is intended as a learning experience and not as a competitor or replacement for any existing Console code. Where it goes and what features get added is up to you.

KISS Konsole is written in C# using the free VS 2008 IDE. The code is heavily commented and aimed at the newbie programmer. It is straight line code with as simple a format as possible.

As a novice C# programmer myself my deep gratitude to Bill, KD5TFD, Dave, WA8YWQ and Joe K5SO for their invaluable assistance in getting KK released. We also owe Phil, N8VB our thanks for making his SharpDSP library available under GPL.

Phil VK6APH

- The code is written in C# using the free Microsoft Visual Studio C# 2008 IDE®
  The code has been successfully tried using Mono on Linux.
- The code is simple linear code and well commented
- The code runs full duplex so you can see/listen to your transmitted signal as well as operate full QSK CW.
- more details here http://openhpsdr.org/wiki/index.php?title=KISS_Konsole
- The GUI has deliberately been made to look as ugly as possible in an attempt to motivate users to improve it!!
- 48/96/192kHz wide bandscope with optional 55MHz wide 'full spectrum' bandscope
- Waterfall display synced to bandscope with AGC option that automatically sets the color of the baseline irrespective of actual band noise levels.
- Fully supports Ozy, Mercury, PennyLane and Hermes. Automatically selects options based on boards present and prompts user for any required setting.
- Checks the release versions of all code in the various boards and
  prompts user when updates are available or required.
- User settings are saved in a simple text file for ease of programming and updating

K.I.S.S. Konsole Project contributors for High Performance Software Defined Radio

- Developed from original code Copyright 2006 © Phil Covington, N8VB

- Phil Harman, VK6APH
- David McQuate WA8YWQ
- Joe Martin K5SO
- George Byrkit K9TRV
- Mark Amos W8XR
- Gordon KA2NLM

New MAC "Heterodyne" software for the OpenHPSDR

by "Jeremy McDermond (NH6Z)" <mcdermj@xenotropic.com>

Heterodyne MAC software here: http://www.nh6z.net/Heterodyne/

http://www.youtube.com/mcdermj

Announced September 7, 2011
Abhi Arounday has created a new LPF/PA/TR board
http://hpsdrhermes.blogspot.com/

*__**15W Amplifier and LPF companion board for Hermes**__*

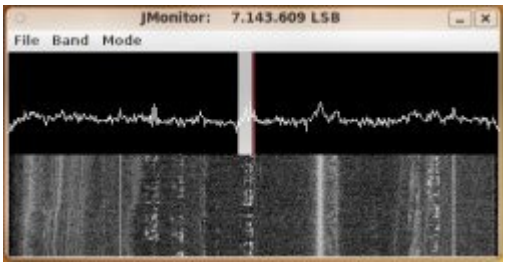
"This Board uses similar logic circuitry as the HPSDR Alex to control the Rx/Tx. switching, LPFs, 3 Antennas, the LPF, SWR bridge are different although 100% compatible with all HPSDR hardware. The amplifier consists of an RD06 driver and a push pull RD15 final which gives out 15W minimum from 160M through 6M, spurious and harmonics are below -40dB on all bands."

http://hpsdrhermes.blogspot.com/

New Hammond box for Hermes by Abhi Arounday
October 8, 2011
http://hpsdrhermes.blogspot.com/

ghpsdr3 Software Developed by John Melton GØORX/N6LYT

http://GØORX.blogspot.com/



John has created a wonderful new light weight "thin client" program called "jmonitor" svn://64.245.179.219/svn/repos_sdr_hpsdr/trunk/N6LYT/ghpsdr3/branches/java/jmonitor that started out with a panadapter spectrum display and now has added a waterfall and full audio demod from the station you are tuned to using his ghspdr server in the UK.
Jmonitor demonstrates the portability and ease of use of the NetBeans IDE, and the subsequent full operation of jmonitor on Windows/XP, Windows-7, Ubuntu Karmic 9.04 and Ubuntu Lucid 10.04. John has also tested jmonitor on his MAC iPhone® and Sun Microsystems Solaris® system. John is currently rewriting his server and plans to offer GTK+ and Qt versions of jmonitor as time allows in the future. A screen capture movie of jmonitor on Windows-7 is located here: http://www.n9vv.com/Images/Hermes/waterfall-demo.mp4

(text from GØORX Blog)
The HPSDR is mounted inside the Antec computer case in a similar may to the article on the Wiki by Ron Cox A complete HPSDR transceiver.

The computer is a PC Chips motherboard with an Intel dual core running at 3.4 GHz with 2 GB of memory. The graphics card is an NVidia GeForce FX5500. The computer is running Ubuntu 9.10 64 bit although it does have an Ubuntu 9.10 32 bit partition that I can dual boot.

To the left of the keyboard is a completed PennyWhistle ready for testing. The large meter on top of the MFJ antenna tuner is a homebrew QRP dummy load and power meter. The meter itself is of surplus Russian origin.

The latest version of ghpsdr now uses a client/server architecture to better support multiple receivers.

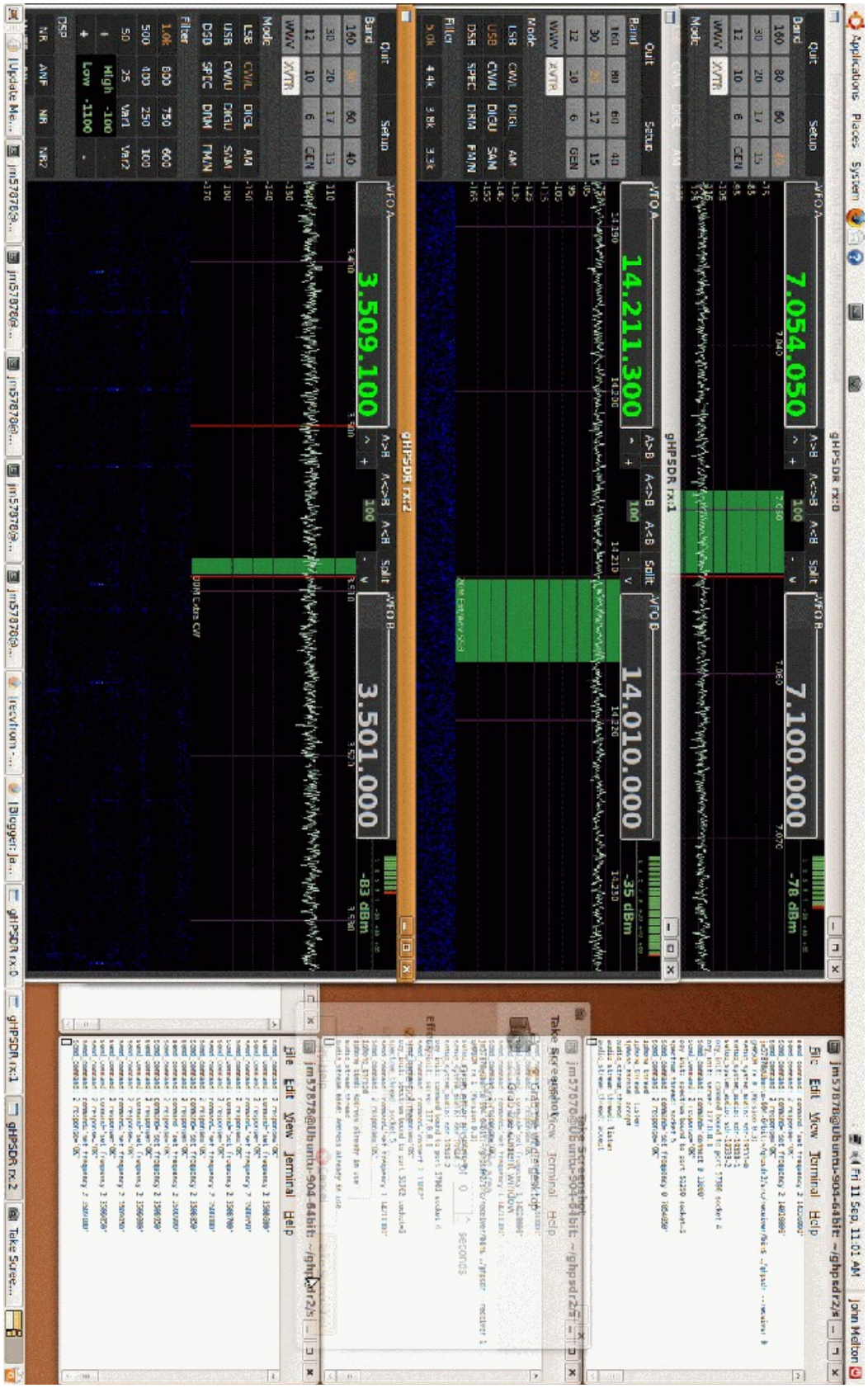
A server application handles the Industry Standard TCP/IP network Ethernet 100BT/1000BT interface to the HPSDR Ozy board.

A client application makes a TCP connection to the server for sending commands to the server. The I/Q stream is sent from the server to the client using UDP.

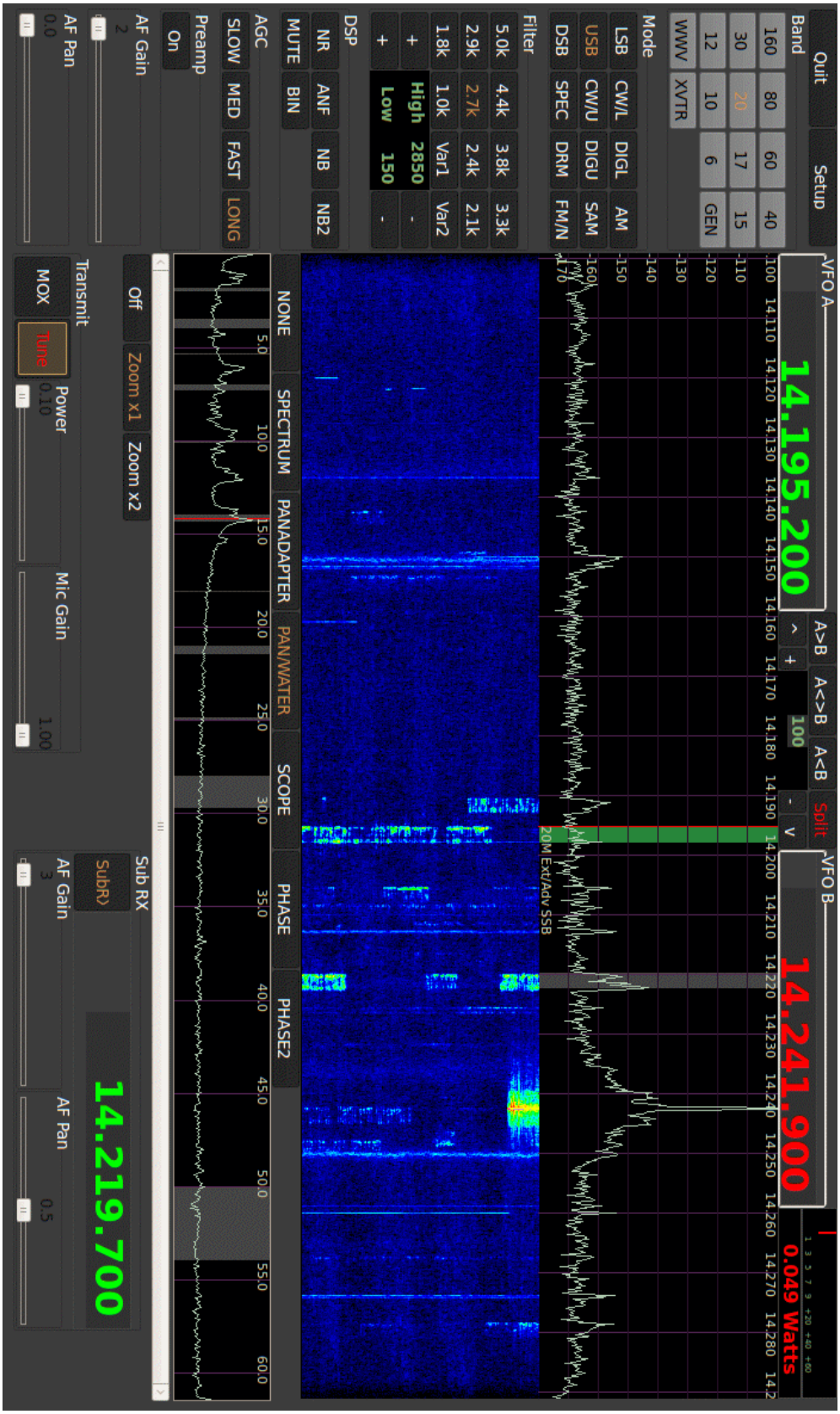
The client can run on the same machine as the server or it can run across the network on another machine. The received audio can either be sent back to the server for playing out of the Mercury card or it can be sent to the local audio.

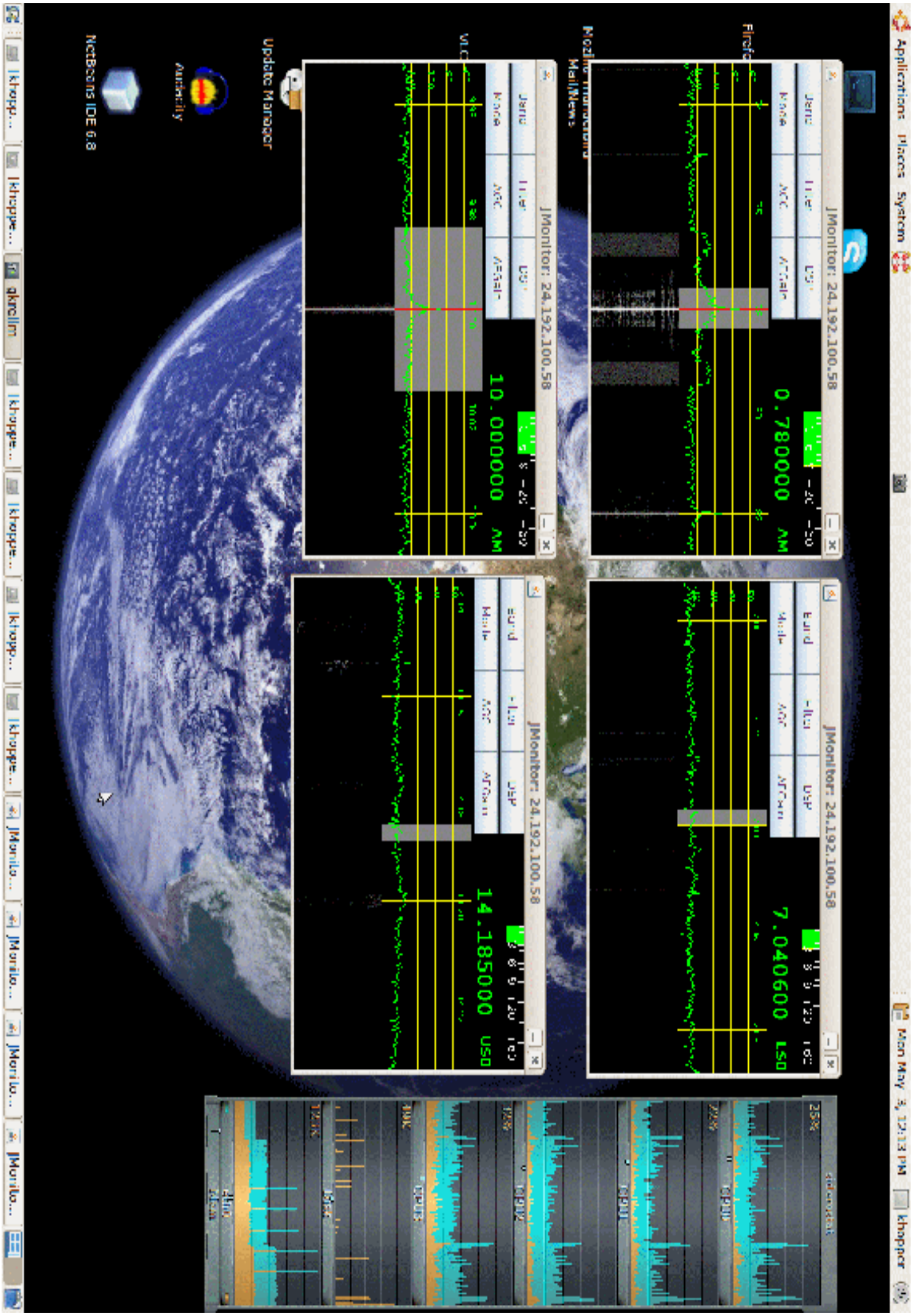
Screen pictures of John's work follows:

John Melton GØORX/N6LYT demonstration – multiple RX on one Mercury board



John Melton GØORX/N6LYT





4 independent simultaneous jmonitor from single Mercury Rx
FPGA code courtesy Bruce W1BW
(photo N9VV Ubuntu 10.04 May 2010)

Appendix A

The CORDIC mathematical algorithm used in the Cyclone-III FPGA

CORDIC - Wikipedia, the free encyclopedia
http://en.wikipedia.org/wiki/CORDIC

CORDIC FAQ
http://www.dspguru.com/dsp/faqs/cordic

CORDIC FAQ-II
http://www.dspguru.com/info/faqs/cordic2.htm

CORDIC for Dummies
http://www.jacques-laporte.org/cordic_for_dummies.htm

The CORDIC Algorithm
http://www.andraka.com/cordic.htm

CORDIC
http://www.nist.gov/dads/HTML/cordic.html

From Hermes FPGA designer Phil Harman VK6APH:

The CORDIC takes the input samples and multiplies them by the sine and cosine of the phase value we feed to it (i.e. the frequency we want to tune to). The CORDIC is a successive approximation approach to generating the sine and cosine of an angle - since it only uses add and shift logic it was used in the early hand-held calculators. If we use enough bits in the CORDIC then the sine and cosine values it generates are so accurate that we get perfect I & Q signals out in terms of how well the amplitudes are matched and how close to 90 degrees apart they are.

As I said it is a successive approximation approach so it takes about 20 iterations to get the accuracy we need. In which case there is a delay of 20/122.88MHz from the time the RF appears at its input to the time the I and Q signals appear.

Because of this delay we use a technique called pipelining - we feed samples into a pipe that is 20 samples long and at the end of the pipe take the result out.

We decimate and filter at the same time. The CIC is a very simple way to produce a filter (just adds and subtracts) so it is very efficient to implement in the FPGA. But it's frequency response is not ideal so we follow it with a CFIR that compensates for the droop in the CIC passband and cleans up the overall shape.

The Hermes FPGA Verilog code can be found on the svn://svn.openhpsdr.org/

Appendix B

Verilog and VHDL

Verilog
http://en.wikipedia.org/wiki/Verilog

Verilog – tutorial learn by example
http://esd.cs.ucr.edu/labs/tutorial/

Verilog by example
http://www.ece.arizona.edu/~ece474a/resources/verilog_tutorial/index.html

================== Verilog programming example ==================

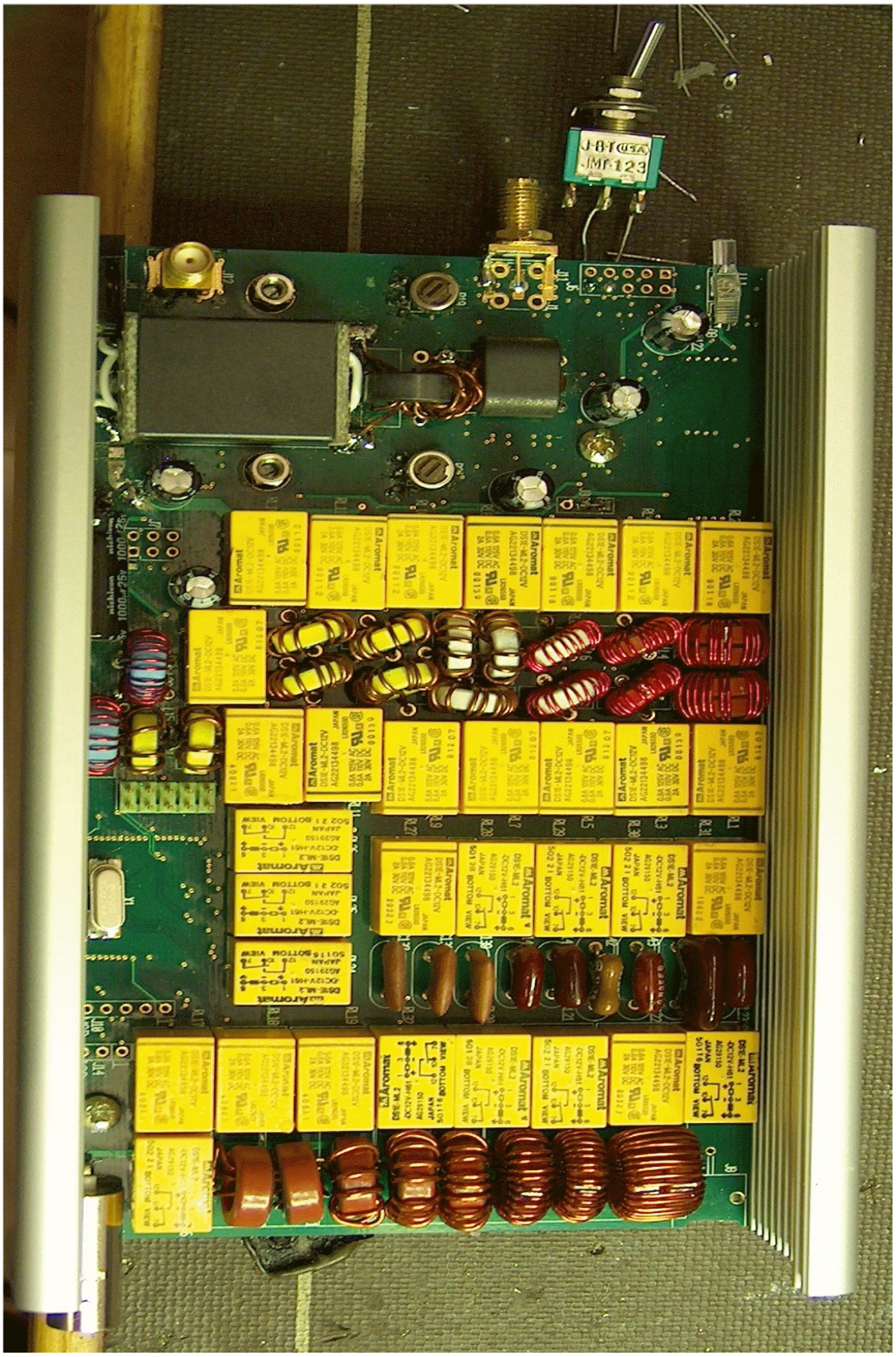
```
// Flash LED to indicate we have a clock selection error

module flash(
             input clock,
             input flag,
             output reg LED);


reg[19:0]error_count;

always @ (posedge clock)
begin
        if (flag) begin
            if (error_count > 1000000)begin
                error_count <= 0;
                LED <= ~LED;                // error so flash LED
                end
            else
                error_count <= error_count + 1'b1;
            end
        else begin LED <= 1'b1;            // no error so LED off
        end
end

endmodule
```

The Hermes FPGA Verilog code can be found on the SVN svn://svn.openhpsdr.org/

Appendix C

Apollo PA prototype in Alpha stage of testing.

photo courtesy Kjell Karlsen - LA2NI
December 18, 2009



note: includes Automatic Tuning Unit when used with Hermes

HERMES FAQ

General

VK6APH first Hermes QSO with ER5GB on 17M December 20, 2009

Q. **What is the Hermes HPSDR Project?**

A. Hermes extends the successful OpenHPSDR Mercury, PennyLane and Atlas on one PCB board with one FPGA. We do not see Hermes as the ultimate project, just a convenient version in a small package. Many will find the small package inconvenient for the add-on like Excalibur or specialized experimentation.

Hermes is designed to be an experimental platform to encourage future development. Hermes is NOT a commercial turn-key product. If you are looking for a full featured out-of-the-box SDR transceiver, you should look at the units from Flex-Radio or similar companies.

caption (click for larger image) photo courtesy Phil Harman VK6APH

Q. **What is the overall architecture of the Hermes Transceiver?**

A. Athena Software Framework <---> Hermes <---> Apollo <---> Antenna <--->

(please refer to the simplified block diagram provided courtesy Phil Harman VK6APH)

In the block diagram (below) you can clearly see the receiver portion depicted on the top of the page and the transmitter section on the bottom half of the page.

Important Hermes features to note:

- Receiver is functionally separate from the transmitter but shares part of the FPGA chip. The receiver runs concurrently and is in FULL DUPLEX with the transmitter portion.
- The Receiver includes both lowpass filtering, attenuation, and preamplification as desired by the operator.
- The transmitter portion has both an output for a transverter and it has the special interface to the Apollo Power Amplifier containing T/R circuitry, lowpass filters and antenna tuner.
- There are 4 voltages needed by various circuits. These are derived from a single 13.8

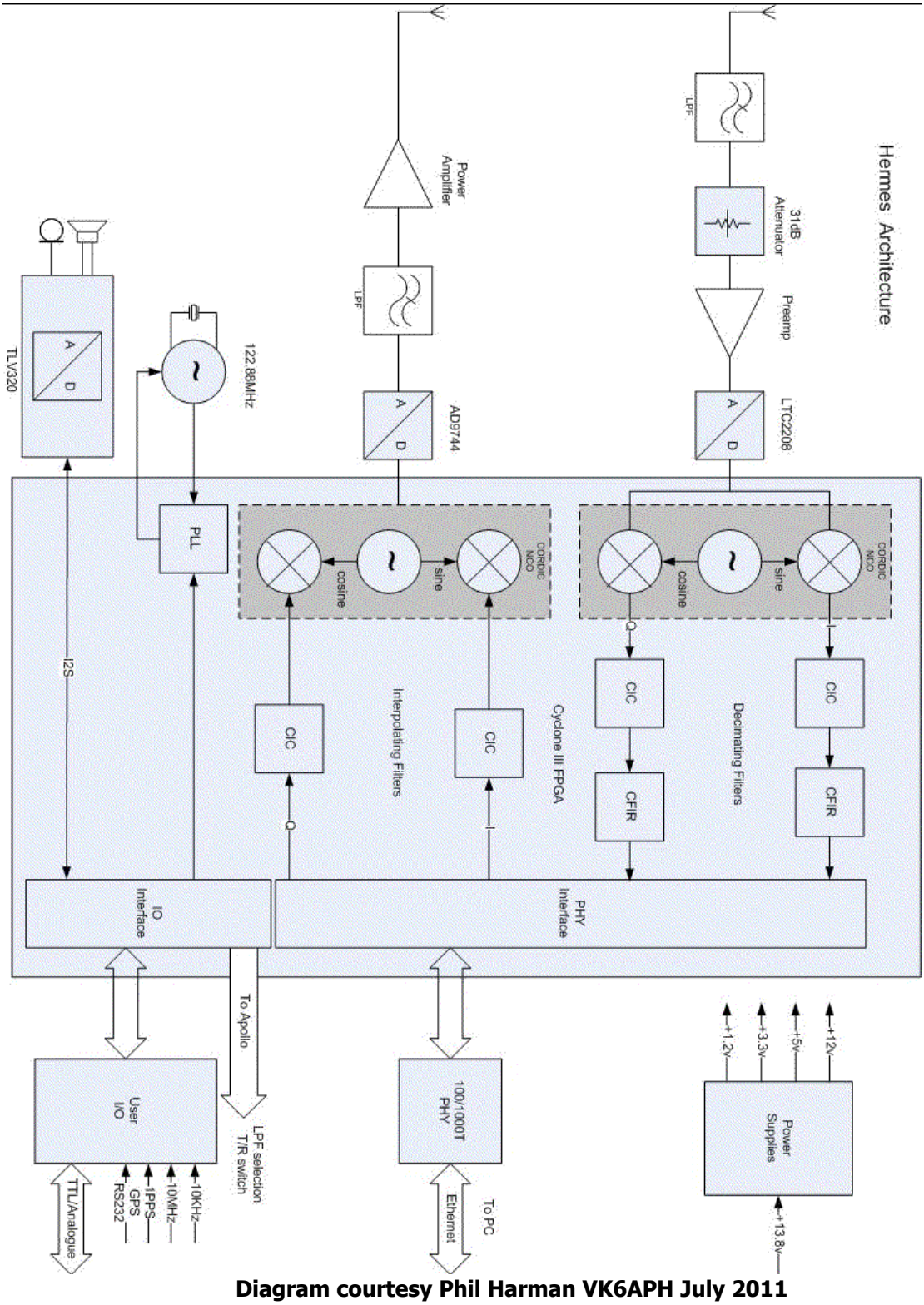


Diagram courtesy Phil Harman VK6APH July 2011

VDC connection (from a common Ham power supply). The switching voltage translation is accomplished by a extremely efficient switching power supply specifically designed for this purpose and included as part of the Hermes PCB.

- The logic elements of the FPGA are configured using Verilog programming. Because the FPGA is such an amazing device, the receiver logical elements and algorithms and the transmitter logical elements and algorithms are able to operate concurrently inside the FPGA chip. In receiving there are Decimating Filters and in the transmitter there are Interpolating Filters.
- The Decimating filters reduce the sample rate from 122.88Msps to 192/96/48ksps as selected by the user. Decimation trades bandscope bandwidth for data rate; the lower data rates are necessary so a standard PC can undertake the rest of the signal processing.
- The Interpolating Filters increase the sample rate from 48ksps to 122.88Msps to comply with the Nyquist criteria.
- Control of the Hermes is provided by the convenient Industry Standard TCP/IP network Ethernet 100BT/1000BT port to a PC. The internal Hermes microprocessor takes care of command and control signals from the PC and responds accordingly.
- 7 user configurable open collector outputs, independently selectable per band and Tx/Rx (for relay control etc - with sequencing via KK software)
- separate open collector PTT connection for amplifier etc control with sequencer.
- Mic PTT jumper selectable from tip or ring connection
- Bias for Electret microphones via jumper
- 4 user configurable 12 bit Analogue inputs (for ALC, SWR etc)
- 3 user configurable digital inputs (for Linear over temp etc)
- Highly efficient switching power supply, less than 330mA (receive) from 13.8 supply rather than wasting heat in an IC regulator.
- I2C bus connector for control of external equipment with full documentation
- Full duplex operation, any split over entire 160m to 6m range
- Full QSK - DSP is not used in PC for CW carrier generation (KK software)
- Up to 8 simultaneous receivers (off one antenna) with suitable PC software.
- Low level transmitter output for transverter use (0dBm) as well as user selectable output attenuator
- Stereo audio outputs at line and headphone levels
- Direct, debounced, connections for CW key (straight or iambic) and PTT
- 122.88MHz master clock can be phase lock to an internal 10MHz TCXO or external reference
- Jumper selectable external reference, with signal processing, to suit numerous GPS locked 10MHz reference sources
- Direct ribbon cable interface to Apollo 20W PA and LPFs or Alex LPFs/HPFs.
  Please see Appendix C for picture of Apollo PA in alpha testing stage.

- Automatic Tuning Unit part of the Apollo design. To be controlled by the special Apollo interface from the Hermes.
- Hermes will support pre-distortion to reach for the best possible transmitted signal.
- Hermes Tx will support ESSB (enhanced SSB) and 6Khz AM limited not by the hardware, but on the software package you are using.

Q. **Who are the contributing members of the Hermes Project?**

A. this truly is an **International collaborative open hardware open software project**

- Kevin Wheatley M0KHZ Project Leader
- Abhi Arunoday PCB layout.
- Phil Harman - VK6APH - Software & hardware development, especially the brain wave for maintaining full DAC bits while reducing power.
- Bill Tracey - KD5TFD - Component sourcing and kitting
- Lyle Johnson - KK7P - significant contributor to PennyLane Tx hardware development
- Scotty Cowling - WA2DFI - Orcad licensing & general advice
- Graham - KE9H - Hermes PA improvements
- Plus numerous others via the reflector.
- Apollo was conceived by Kjell Karlsen - LA2NI

Q. **Where is the Hermes Project Wiki?**

A. see HERMES

Q. **What is the History of the Hermes Project?**

A. http://openhpsdr.org/hermes.html

Hermes - A proposed DUC/DDC Transceiver

Project Leader: Kevin M0KHZ

Following the outstanding success of Mercury and PennyLane, and while investigating the verilog code for both, I had the insane idea of merging the Verilog code of Mercury and PennyLane into a single FPGA! I played around with this idea for a while and the more I thought about it the more I liked the idea.

So here is the proposal, to develop a single board HPSDR based on the hardware of Mercury and PennyLane and a single large FPGA.

This board would have PC connectivity by Industry Standard TCP/IP network Ethernet 100BT/1000BT. I'm planning to squeeze this all onto EuroCard sized PCB (100 x 160 mm), and if I utilize both sides I might even have room for a Pennywhistle type PA :-).

Q. **What are the Objectives of the Hermes Project?**

A. http://openhpsdr.org/hermes.html Hermes is simply the Mercury, PennyLane and Atlas on one board with one FPGA. It also includes the signal processing circuitry from Excalibur so an external 10MHz reference (which can be GPS locked) can be used.

We do not see Hermes as the ultimate project, just a convenient version in a small package. Since there is no equivalent to the Atlas bus it does not support the expansions capabilities of Mercury. PennyLane etc.

Hermes is designed to be an experimental platform to encourage future development. Hermes is NOT a commercial turn-key product. If you are looking for a full featured out-of-the-box SDR transceiver, you should look at the units from Flex-Radio or similar companies.

Q. **How does the Hermes architecture work?**

A. please refer to Hermes

The architecture of the system uses state-of-the-art digital electronics to accomplish **three** main functions:

1. Digital Down Conversion from RF frequencies to baseband for mathematical manipulation(DDC).
2. Digital Up Conversion from audio frequencies to RF frequencies (DUC) for transmission.
3. Modulation (Tx) and Demodulation (Rx), DSP, AGC, Filtering, Noise Blankers, band selection and all the features of a modern transceiver - accomplished by the Computer program on the Industry Standard TCP/IP network Ethernet 100BT/1000BT connected Personal Computer.

    - Initially software is being developed by John Melton for Linux and by Phil Harman for Windows. The Flex Radio PowerSDR™ software will also continue to be supported for HPSDR. The specific computer languages don't matter to you unless you are interested in portability among platforms, or perhaps adding your favorite new feature.

    - All this is accomplished using a single PCB (Hermes) and the associated firmware for the FPGA and software for the PC.

    - The PC software may be split into a "server" connected to the Hermes via Industry Standard TCP/IP network Ethernet 100BT/1000BT and a "client" Graphical User Interface that runs remotely over the Internet. The net might be inside a single PC, or across the room in your shack, or across the Globe in another country. It will be great fun to see these applications appear and mature over time. This is part of the Hermes Experimental experience.

    - Hermes is a great success story that begins with the robust OpenHPSDR system on the Atlas backplane (motherboard). Hermes stands on the shoulders of Mercury(Rx), PennyLane(Tx), Pennywhistle(PA), Metis(Control and Interface), and the suite of boards offered to the experimenter in the HPSDR arena.

    - Just as OpenHPSDR offers a full transceiver using DDC/DUC, Hermes will offer similar functions at a lower entry price point and in a smaller configuration. The software is being designed to be functionally similar for both systems.

Q. **Where is the software and firmware for Hermes?**

A. The proposed OpenHPSDR Hermes Graphical User Interface software implementations are:

- PowerSDR™ Flex-Radio Corporation with KD5TFD mods.
- KISS Konsole Beautiful C# fundamentals by Phil Harman VK6APH.
- Ghpsdr John Melton GØORX/N6LYT designed for Linux.

- Athena Software Framework proposed by Dave KV0S.

- The "firmware" commands for the FPGA, ADC, and DAC should be loaded automatically or stored in non-volatile memory chips in the system. Firmware may be uploaded easily with the built in (on board) updating firmware via Industry Standard TCP/IP network Ethernet 100BT/1000BT.

Resources

Q. **Where is the OpenHPSDR mailing list?**

A. Please follow these links to the archives, subscription information and main webpage.

- http://lists.openhpsdr.org/pipermail/hpsdr-openhpsdr.org/ archives

- http://lists.openhpsdr.org/listinfo.cgi/hpsdr-openhpsdr.org subscriptions

- http://openhpsdr.org/ main organization webpage

Q. **Who do I call for help?**

A. The group helps each other via the HPSDR email list. In the future there may be more frequent use of the "Teamspeak" Voice over IP technology to provide interactive help as well.

Q. **Where are the schematics?**

A. Schematics are being published as they are solidified and then when the production boards are manufactured.

Q. **Where are the board layout files?**

A. Board layout diagrams will be made available as Hermes moves closer to production.

Q. **Where are the Verilog files?**

A. The FPGA Verilog files will be stored in the SVN (SubVersion Repository) as they are made available.

Q. **Where is the Users Manual?**

A. (to be developed)

Q. **Where is the Builders Manual?**

A. The Hermes boards will be pre-built (manufactured) due to the complexity of the Surface Mount Technology and the difficulty of home soldering (0.5mm lead centers). At this time no Builders Manual is outlined. However as Apollo or other boards are married to Hermes it may be appropriate to have a Builders Manual with suggestions for successful chassis layout and connectors.

Q. **Where is the Troubleshooting Guide?**

A. (to be developed)

Q. **Is there an in-depth technical manual?**

A. (to be developed)

Q. **Where can I get the orientation and training DVD?**

A. To learn all about Digital Down Converter technology, please purchase DVD #6 from (Amateur Radio Video News) in which Phil Harman VK6APH teaches us the practical details from his wonderful presentation at DCC-2008. The DVD consists of 4 hours of education in DDC by Phil Harman. The ARVN webpage says:

> Software Defined Radio
> "Through the Looking Glass"
> Phil Harman VK6APH leads you on an entertaining, detailed trip through the design of the Mercury SDR receiver. With the A/D converter preceded only by a bandpass filter, Mercury does everything in software, at a price hams can afford. It is the leading edge in ham radio technology.
> http://www.arvideonews.com/dcc2008/

Q. **Where can I get a power point presentation for my club meeting?**

A. (to be developed)

Q. **Is there an online Internet Hermes/Apollo radio for me to control remotely?**

A. When the server and client (GUI) software is properly separated and tested, there should be several systems on the Internet to test. We are all looking forward to those experiments.

Q. **Where is the Teamspeak voice over Internet activity?**

A.

- http://www.teamspeak.com/ Teamspeak download website
- 174.132.74.55:9274 OpenHPSDR Teamspeak IP address
- Reference to the Teamspeak Users Installation Guide (pdf)

Q. **Why did OpenHPSDR decide to make this an Open Source design?**

A. The whole HPSDR project has followed the community spirit of sharing and making contributions whenever and wherever you can. **This is a not-for-profit adventure**. There are no paid employees and only the cost of design and manufacture are recovered in the price of the boards.

- OpenSource dot org
- Wikipedia topic OpenSource Software

Technical

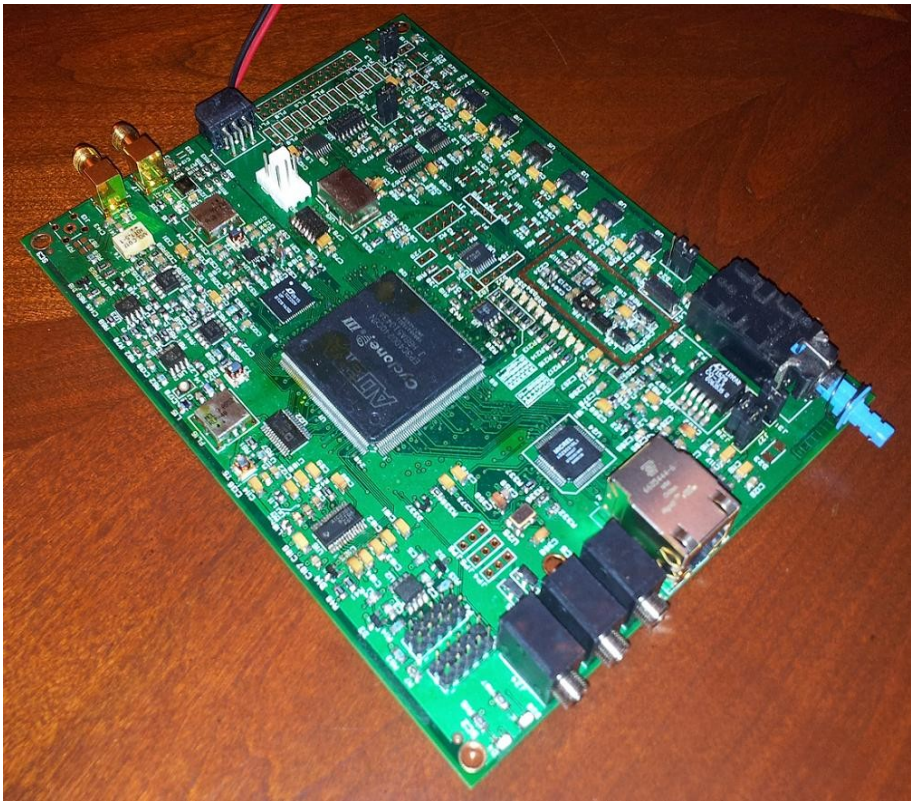


photo courtesy *Abhi Arunoday*

Q. **What is a DDC receiver see Mercury?**

A. DDC is the abbreviation for the term Digital Down Conversion. DDC receivers are able to finally fulfill the dream that has been expressed in Ham Radio magazines for 50 years – to place the digital processing of analog RF information closer to the antenna. The OpenHPSDR Mercury receiver accomplishes that goal. In the OpenHPSDR Mercury and Hermes projects, the antenna is connected to a modern integrated circuit chip. The chip in this case is a **very** fast Analog to Digital conversion device called the LTC2208. The Mercury and Hermes designs are designed to be supplemented by bandpass, attenuation, and pre-amp circuits.

Q.**How does the ADC (Analog to Digital) chip work?**

A. The Linear Technologies 2208 is a high speed, state-of-the-art, Analog to Digital conversion integrated circuit. The specifications for the LTC2208 can be found on the Linear Technologies website.

The LTC-2208 illustrates the beginning of a most exciting new era in Ham Radio. These ADC's offers us the ability to directly convert analog RF signals to digital signals. The purpose is to get I and Q digital signals from which we can decode virtually any modulated signal. Analog I and Q signals lack the precision and malleability of their precise digital cousins.

The conversions happen in the HPSDR Mercury and Hermes at the blazing rate of 125 Million Samples Per Second! I realize that this is a difficult concept to grasp. There is a great deal of helpful material available on the Internet and from various magazines and books. The ARRL DSP book written by Doug Smith KF6DX has several chapters devoted to various aspects of digit-

al sampling of analog signals. Again, the objective is to create digital representations of the RF band of interest so that it can be further processed by innovative and complex modern computer technologies.

New Linear Technologies devices allow experimenters to build affordable equipment that processes the digital representation of the entire RF spectrum throughout the HF bands (.05Mhz through 55Mhz). Digital processing gives us extraordinary demodulation, digital signal processing, filters, AGC methods, and signal handling that is far beyond the capability any of our older analog circuit designs.

In the analog I/Q world of the Phasing method, the precision of the analog components limited opposite sideband rejection to one half the value achieved in the HPSDR suite. The software doesn't change values as equipment heats up and something as critical as image rejection is always at it's mathematically optimum value.

The ability of the LTC-2208 to sustain 125 million samples per second couples it to various algebraic and mathematical methods that are processed easily inside a miniature computer like the Cyclone-III FPGA. A CW signal on 3.552Mhz appears on the output pins of the LTC-2208 among the stream of discrete numerical values ranging from -32768 to +32767. The LTC-2208 converts the RF impulses to decimal values using all sixteen bits of it's internal circuitry. Various DDC receiver products are on the market using 12, 14, and 16 bit ADC chips. They all work well and have unique receiver characteristics based on their ADC construction. Perhaps in the coming decade we will see even higher precision ADC chips that are within the experimenters price range.

During every tick of your wall clock, the LTC-2208 presents one hundred and twenty five million samples of the RF spectrum at it's output pins. Each numerical sample is an aggregate value of the RF energy throughout the HF spectrum. It is the job of the logic elements in the Cyclone III FPGA to create I and Q digital representations of the RF data, interpret, separate, filter, convert, and prepare the numerical values so that they can be post-processed by the computer technologies such as suggested in the Athena software framework. The Athena software framework proposal will convert the numerical data back into human viewable form using the magic of DSP and Fourier transforms. The digital signals from the LTC-2208 are passed without interference to the Cyclone-III FPGA in a continuous stream where they are processed in real time.

With a little study, you will see that terminology such as "time domain" and "frequency domain" will easily be related to oscilloscope patterns that we are all familiar with. In addition to the ARRL DSP book, another popular text is The Scientist and Engineer's Guide to Digital Signal Processing By Steven W. Smith, Ph.D.

Q. **What is a DUC transmitter or exciter?**

A. (to be developed)

Q. **What is the designed output power of the Hermes PA?**

A. If Hermes is used by itself then the output power is 500mW PEP. If used in conjunction with Apollo PA, lowpass, and T/R board this is designed to produce 10W - 20W output. Technical Tx specifications will be included here in the FAQ as they are made available.

Q. **Is the Hermes designed to be FULL DUPLEX?**

A. *YES* and cross band from any band to another!

Q. **Will the Hermes Tx allow Enhanced SBB (ESSB) or 6Khz AM transmission?**

A. Yes, the Hermes hardware does not restrict the bandwidth of the transmitted signal. If your PC supporting software can generate ESSB or 6Khz AM, then your Hermes will do it.

Q. **What are the Hermes performance specifications?**

A. (to be developed)

Q. **What is the function of the Cyclone FPGA Chip?**

A. FPGA is the abbreviation for a **Field Programmable Gate Array**. One of the best discussions about FPGA's is on the Wikipedia. An FPGA is a reconfigurable and programmable set of basic logic elements like gates. All the computers (CPU's) that we use have similar basic logic elements at their most detailed level. Wikipedia says that applications of FPGA's include digital signal processing, software defined radio, aerospace, defense systems, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, and computer hardware emulation. Fortunately, the exciting complexity and reconfigurability of these logic elements can be expressed in human readable form by using a Hardware Description (programming) Language from Verilog(R) called VHDL.

Q. **What is the "CORDIC" algorithm?**

A. The CORDIC algorithm programmed into the Cyclone-III FPGA generates a digital representation of the I and Q data needed for further modulation and demodulation by the accompanying PC.

(from the Wikipedia webpage CORDIC)

CORDIC **CO**ordinate **R**otation **DI**gital **C**omputer is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It is commonly used when no hardware multiplier is available (e.g., simple microcontrollers and FPGAs) as the only operations it requires are addition, subtraction, bitshift and table lookup.

The modern CORDIC algorithm was first described in 1959 by Jack E. Volder. It was developed at the aeroelectronics department of Convair to replace the analog resolver in the B-58 bomber's navigation computer,[1] although it is similar to techniques published by Henry Briggs as early as 1624. John Stephen Walther at Hewlett-Packard further generalized the algorithm, allowing it to calculate hyperbolic and exponential functions, logarithms, multiplications, divisions, and square roots.

Originally, CORDIC was implemented using the binary numeral system. In the 1970s, decimal CORDIC became widely used in pocket calculators, most of which operate in binary-coded-decimal (BCD) rather than binary. CORDIC is particularly well-suited for handheld calculators, an application for which cost (eg, chip gate count has to be minimized) is much more important than is speed. Also the CORDIC subroutines for trigonometric and hyperbolic functions can share most of their code.

Some good web references are:

- http://www.itl.nist.gov/div897/sqg/dads/HTML/cordic.html
- http://www.andraka.com/cordic.htm
- http://www.jacques-laporte.org/cordic_for_dummies.htm
- http://www.dspguru.com/dsp/faqs/cordic
- http://en.wikipedia.org/wiki/CORDIC

Q. **How do signals get from the Analog (RF) to the Digital (I/Q) domain?**

A. Please read the discussion above about the LTC2208 ADC and the operation of the Altera Cyclone-III FPGA chips. [this answer will be expanded in the future]

Q. **How do analog (microphone) signals get to the digital domain?**

A. Please read the discussion above about the LTC2208 ADC and the operation of the Altera Cyclone-III FPGA chips. [this answer will be expanded in the future]

Q. **What are the three "Generations" of SDR technology?**

A. The three "Generations" are:

1. the Analog Phasing method
2. the "Tayloe" or QSD (Quadrature Sampling Detector/mixer)
3. the Direct Down Conversion (DDC/ADC) method

Q. **Are there any other Generation-III transceivers?**

A. Yes there are several that have appeared in various magazines:

- The full HPSDR Atlas + Mercury(Rx) + Pennywhistle(Tx) OpenHPSDR
- Peter Martinez G3PLX RADCOM March 2009
- I0CG SDRx Rx/Tx
- Ettus Research LLC USRP2
- ADT-200A by Hans HB9CBU
- "HiQSDR" designed by N2ADR published in QEX

Q. **What is the purpose of the I2C bus in the Hermes project?**

A. It's primary use is to send the currently tuned frequency to the Automatic ATU on Apollo. It can also be used to control external I2C peripherals.

Q. **Where is the Rx and Tx Image Rejection adjustment?**

A. Operator image rejection adjustment is **NOT** required with a DDC base transceiver. The reason one has to deal with image rejection on QSD/QSE is because the I/Q signal is in the analog domain and the two analog channels are always slightly different. The perfect quadrature relationship between IQ cannot be maintained since the I and Q analog channels will always be slightly different from each other - just the nature of having two different analog channels. PowerSDR from Flex deals with the image rejection using a sophisticated algorithm.

In the DDC/DUC architecture you don't have IQ in the analog domain, just a plain real signals. The I/Q decimation all happens in the digital domain - since it's all math, there's no difference between the I and Q channel processing so there are no image issues. This is not to say it's perfect ... it's only as perfect as the number of bits used in the processing and A/D and D/A channels and a properly constructed FPGA code base. [above description generously contributed: by Bill KD5TFD, Phil VK6APH, and Bob N4HY]

Q. **Is the Hermes transceiver reverse polarity protected?**

A. Yes, there is protection in the power supply and on each board. Of course the builder should take every possible protection to insure that the power supply is connected properly.

Q. **Where is the QSD that I see in so many other SDR designs?**

A. There is no Quadrature Sampling Detector or Mixer in the Hermes design. All that work is done with clever mathematics inside the Cyclone FPGA chip using the digitized RF directly from the LTC-2208 Analog to Digital (ADC) chip connected to the antenna (via bandpass/preamp).

Q. **What is the Dynamic Range of the Hermes (Mercury) receiver?**

A. (to be determined and published)

Q. **What is Undersampling?**

A. Undersampling is a method used to reach into the VHF/UHF spectrum with the Hermes receiver.

Q. **What power supply is recommended?**

A. A standard 13.8VDC supply is the design goal. More information will be published as the various Hermes components are assembled and tested.

Q. **What High Voltage MOSFET's are used in the (Apollo) Power Amplifier?**

A. The PA in Apollo is based in the successful Pennywhistle design - see that schematic for more details or the current Apollo schematic on this Wiki Apollo

Q. **Does Hermes include a "Class-A" bias adjustment?**

A. No, the 500mW PA on Hermes operates in Class AB. With a suitable heatsink Apollo could be operated in Class A if required

Q. **What commercial Linear Amplifiers will Hermes work with?**

A. Since the basic Hermes board produces 500mW an intermediate PA will be required (e.g. Apollo or Pennywhistle) to increase this to a level suitable for driving a commercial Linear. At the 20W PEP level there are numerious amplifers that could be use. Hermes provides dedicated PTT outputs for driving switching a linear as well as seven open collector outputs that, via the PC GUI, can be used to select LPFs, antennas etc.

Q. **What is pre-distortion and why is it important to DUC transmitters?**

A. Yes, Hermes (as well as Penny) can do pre-distortion since we run full duplex. It is beyond Class A - basically what you do is listen to your Tx signal and compare it to the {ideal} signal you are creating (i.e. your I&Q signals). If they differ then you can 'pre-distort' the I&Q signals so that when it is distorted {modified} in the PA, the result is a linear system. All cell phone Tx use this technique.

Q. **Can Hermes operate in the VHF/UHF spectrum?**

A. The Hermes Tx is specifically designed to include a 0dBm output suitable for a transverter. Many other solutions are expected when the Hermes reaches production status.

Q. **How much data can I expect to pump through a Industry Standard TCP/IP network Ethernet 100BT/1000BT?**

A. Industry Standard TCP/IP network Ethernet 100BT/1000BT is specified at 100mbps or 1000mbps (1Gigabit) per second. This needs to be split between transmit and receive. On receive, independent tests have shown as sustained transfer rate of > 35Mbytes per second. This is sufficient to support eight 192KHz wide receivers in real time.

Q. **Is there a Linux version of the server and GUI?**

A. Yes, John Melton GØORX/N6LYT is working on both a GTK+ and C++/Qt version for Linux platforms.

Q. **Is there an iMAC version of the server and GUI?**

A. Not at this time, however there is a large MAC HPSDR community and a port of one of the software suits is expected shortly.

Apollo

Q. **What is the Apollo part of the OpenHPSDR project?"**

caption (click for larger image) photo courtesy Kjell Karlsen - LA2NI

A. see: APOLLO APOLLO is to be a companion 15W PA, Low Pass Filter and T/R switching (PIN or relay) for Hermes. The idea is to build a self contained HPSDR Transceiver into a box similar to the one used for the two Alex boards.

The box, made by Hammond has a sliding cover on one of the sides (Series 1455, PN 1455N1601). This cover can be used as Front Panel and behind this a display up to 4 inches may be installed. There will also be space for a controller (Beagleboard or something else). One of the goals is a small platform to use as controllers for a self contained transceiver.

Another goal is current consumption of less than 0,3- 0,4 A on Receive and, based on measurements on the Alpha PCB, looks achievable. Using latching relays for LPF switching will save power. The interface to Hermes will be via SPI and I2C.

The LP Filters will be based on Alex but with only one Antenna connector. The toroids may be smaller (T38 instead of T50). Also the capacitors can have lower voltage ratings. An Antenna Tuner will also be implemented.

Q. **What is the Apollo board and do I need it?**

A. Apollo Discussion

Q. **How is the Apollo board integrated or connected to the Hermes transceiver?**

A. Via an 10 pin and 5 pin ICD ribbon cable.

Commercial Sales prohibited

Q. **Who sells the OpenHPSDR boards?**

A.This has yet to be decided. Hermes will initially be licensed under the non-commercial licences NCL License

Q. **Can I build it into my own enclosure (chassis)?**

A. Yes. The design is flexible and you are encouraged to build Hermes into whatever configuration pleases you. HPSDR hopes to offer a chassis for Hermes that will be pre-punched for all the attachments and connectors.

Q. **Can I build Hermes into my own OEM product for sale?**

A. No, the open hardware license allows you to build and enjoy the Hermes transceiver, however you may not build your own commercial product using the HPSDR copyrighted boards and design.

Q. **How are the Hermes hardware and software legally protected?**

A. Yes, Hermes will initially be licensed under the non-commercial licences NCL License

Q. **Is your Intellectual Property copyrighted or otherwise protected?**

A. Yes

Q. **Can I purchase bare boards and populate them myself?**

A. Yet to be determined. [this answer will be expanded in the future]

Q. **Can I buy the chips individually?**

A. Yes but they are very expensive in small qualities from the manufactures

Q. **Do you have a European distributor or dealer?**

A. No for Hermes at this point. Some **HPSDR** boards are available from vendors in Europe. See manufactures links

Q. **Do you have an .AU or .NZ distributor or dealer?**

A. No

Compare to other SDR designs

Q. **How is Hermes/Apollo different from the Flex-Radio(c) 5000, 3000, and 1500?**

A. Hermes is a Generation-III SDR DDC/DUC design exceeding all Generation-II QSD capabilities.

Q. **What is the difference between the Hermes Mercury DDC Rx and the QuickSilver from Phil N8VB Software Radio Laboratory LLC?**

A. The Hermes is a smaller more compact version of the wildly successful Atlas backplane and OpenHPSDR add-on HPSDR boards.

How Do I

Q. **Operating SSB**

A. (operating aid information to be developed) [this answer will be expanded in the future]

Q. **Operating MARS**

A. (operating aid information to be developed) [this answer will be expanded in the future]

Q. **Operating CW**

A. (operating aid information to be developed) [this answer will be expanded in the future]

Q. **Will Hermes be a truly "TOR" capable QSK CW rig? (where ARRL defines TOR = T/R time < 20ms)**

A. Yes. Hermes operates in full duplex at all times. TOR operation depends on external factors such as T/R relay switching times and PC code latency.

Q. **Will Hermes operate on popular digital modes such as PSK31, ALE, and EasyPal digital SSTV?**

A. Yes, like the other OpenHPSDR boards, Hermes uses I and Q baseband data to modulate and demodulate signals. Subject to bandwidth limitations (currently 192kHz on receive and 5kHz on transmit - these can be altered by changing FPGA code) and Industry Standard TCP/IP network Ethernet 100BT/1000BT data rates any current or future data mode can be used.

Q. **Connect to a Linear Amplifier**

A. Hermes provides a dedicated open collector PTT as well as seven general purpose open collector outputs for interfacing a linear amplifier. In addition, four 12 bit analogue inputs are provided that, via suitable signal conditioning, can be used to monitor amplifier parameters e.g. forward power, temperature etc.

Q. **Operating with a Transverter**

A. Hermes provides two low level transverter outputs, one at 0mW max and the other at 500mW max. The 500mW output can be connected to an ob-board power divider, and hence to a dedicated SMA output, to enable the user to select an output below this level. A dedicated open collector PTT and seven open collector outputs can be used (with sequencing via a suitable PC GUI e.g. KISS Konsole) for transverter control.

Q. **Can I record audio data**

A. This feature is provided by the Flex PowerSDR(TM) Windows software.

IMPORTANT
Hermes provides a stereo Audio Amplifier suitable for driving speakers from 3 to 8 ohms. The amplifiers are implement in a bridge configuration so that one side of the speaker must NOT be connected to earth or 0v. Connect the Left speaker to pins 1 and 2 of J16 (or Tip and Ring of J21) and the Right speaker to pins 1 and 2 of J15 (or Tip and Ring of J22).

Q. **Can I record I/Q (RF) data?**

A. This feature is provided by the Flex PowerSDR(TM) Windows software.

Q. **How do I record Rx audio for later playback?**

A. This feature is provided by the Flex PowerSDR(TM) Windows software.

Software

Q. **How do multiple receiver channels work?**

A. The FPGA used by Hermes is currently the largest (in terms of number of available gates) leaded device presently available. Since the FPGA code for the transmitter, one receiver etc occupies only 50% of the device there is room for some seven additional receivers. Since each of these receivers share the one ADC then they all share the same antenna. Hence, to monitor multiple bands simultaneously a multi-band antenna (e.g. trap vertical) or some form of diplexer will be required.

Suitable PC software John Melton can be used to configure, and display, multiple receivers.

Q. **Can the Flex-Radio(R) PowerSDR(c) be used with Hermes?**

A. Yes, Bill KD5TFD has maintained the OpenHPSDR version of PowerSDR.

Q. **What is the K.I.S.S. Konsole?**

A. K.I.S.S (Keep It Simple Stupid) Konsole is a straightforward PC program that will allow beginners in SDR and DSP programming to get their feet wet.

KK is intended as a learning experience and not as a competitor or replacement for any existing Console code. Where it goes and what features get added is up to you.

KISS Konsole is written in C# using the free VS 2008 IDE. The code is heavily commented and aimed at the newbie programmer. It is straight line code with as simple a format as possible.

As a novice C# programmer myself my deep gratitude to Bill, KD5TFD, Dave, WA8YWQ and Joe K5SO for their invaluable assistance in getting KK released. We also owe Phil, N8VB our thanks for making his SharpDSP library available under GPL. by Phil VK6APH.

K.I.S.S. Konsole for High Performance Software Defined Radio Developed from original code Copyright 2006 (C) Phil Covington, N8VB

K.I.S.S. Team Members

- Phil Harman, VK6APH
- David McQuate WA8YWQ
- Joe Martin K5SO
- George Byrkit K9TRV
- Mark Amos W8XR
- Gordon, KA2NLM

Q. **How is Hermes software different from PowerSDR(c)?**

A. It only supports OpenHPSDR hardware and provides basic receiver and transmitter functions. It does not have the rich features of PowerSDR.

Q. **What have you changed in the Dttsp module?**

A. KK software uses the SharpDSP routines written by Phil Covington N8VB.

Q. **How do I add a feature to the GUI?**

A. Which GUI?

Q. **How wide is the panadapter (spectrum) display?**

A. 55MHz fixed and simultaneously user selectable 48, 96 or 192kHz.

Q. **Will the Hermes server and GUI work remotely from each other across the Internet?**

A. Some proposed and experimental software is being developed with a server/client model.

Q. **Will Hermes server and GUI work on WindowsXP, Vista, Windows-7?**

A. Software development is happening at a quick pace. Watch the HPSDR email list for announcements from the volunteer authors.

Ordering and Support

Q. **How do I order the Hermes board?**

A. (to be determined) [this answer will be expanded in the future]

Q. **What is the Warranty period?**

A. (to be determined) [this answer will be expanded in the future]

Q. **What does the warranty cover?**

A. (to be determined) [this answer will be expanded in the future]

Q. **What support is available?**

A. (to be determined) [this answer will be expanded in the future]

Q. **Can I subscribe to future upgrades and support options?**

A. (to be determined) [this answer will be expanded in the future]

Q. **What shipping and insurance options are available?**

A. (to be determined) [this answer will be expanded in the future]

Q. **How do I avoid the excessive "VAT" tax in my country?**

A. (to be determined) [this answer will be expanded in the future]

Q. **Do you accept payment via PayPal(R)?**

A. (to be determined) [this answer will be expanded in the future]

Future plans for HPSDR

Q. **How can I contribute to the future success of the** HPSDR **project?**

A. Several projects are are being proposed and developed all the time. Subscribe to the reflector, listen to teamspeak, read the website and the Wiki pages.

Q. **I am a talented programmer, how can I help?**

A. Several projects are are being proposed and developed all the time. Subscribe to the reflector, listen to teamspeak, read the website and the Wiki pages.

Q. **What are the future plans for the OpenHPSDR Project?**

A. Several projects are are being proposed and developed all the time. Subscribe to the reflector, listen to teamspeak, read the website and the Wiki pages.

NOTES

http://kc.flex-radio.com/KnowledgebaseArticle50028.aspx?Keywords=K5SDR+article

http://kc.flex-radio.com/KnowledgebaseArticle50027.aspx?Keywords=K5SDR+article

http://kc.flex-radio.com/KnowledgebaseArticle50025.aspx?Keywords=K5SDR+article

http://kc.flex-radio.com/KnowledgebaseArticle50026.aspx?Keywords=K5SDR+article

Linrad: New Possibilities for the Communications Experimenter Part 1 (237422 bytes, PDF file) Discussion opens with analog versus digital RF-input techniques and attendant performance considerations. QEX Nov/Dec 2002. p 37-41.

Linrad: New Possibilities for the Communications Experimenter Part 2 (923583 bytes, PDF file) From the Analog World into the Digital: How do we get the desired signal from RF to the sound card ? QEX Jan/Feb 2003. p 41-48.

Linrad: New Possibilities for the Communications Experimenter Part 3 (396080 bytes, PDF file) Linux and the Linrad software package. QEX May/June 2003. p 36-43

Linrad: New Possibilities for the Communications Experimenter Part 4 (752789 bytes, PDF file) Examples of simple Linrad use with an amateur transceiver (IC706) yield improved noise blanking and filtering. QEX Sept/Oct 2003. p 29-37

Linrad with high performance hardware. (518802 bytes, PDF file) Together with the WSE RX converters. Linrad is a software-defined receiver that should exceed any other receiver in dynamic-range performance. QEX Jan/Feb 2004. p 20-31

http://gnuradio.org/redmine/attachments/129/USRP_Documentation.pdf

http://gnuradio.org/redmine/wiki/gnuradio/UsrpRfxDiagrams

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